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Strategies for Fast-Switching in All-Polymer Field Effect Transistors

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Low-cost printable field effect transistors (FETs) are typically associated with slow switching characteristics. Dynamic response of polymer field effect transistors (PFETs) is a manifestation of time scales involved in processes such as dielectric polarization, structural relaxation, and transport via disordered-interfacial states. A range of dielectrics and semiconductors are studied to arrive at a parameter which serves as a figure of merit and quantifies the different processes contributing to the switching response. A cross-over from transport limiting factors to dielectric limiting factors in the dynamics of PFETs is observed. The dielectric limited regime in the PFET dynamics is tapped in to explore high speed processes, and an enhancement of switching speed by three orders of magnitude (from 300 µs to 400 ns) is observed at channel lengths which can be accessed by low cost printing methods. The device structure utilizes polymer-ferroelectrics (FE) as the dielectric layer and involves a fabrication-procedure which assists in circumventing the slow dynamics within the bulk of FE. This method of enhancing the dynamic response of PFETs is universally applicable to all classes of disordered-FE.

1. Introduction

Low-cost, large-area, solution-processing and roll-to-roll printing of polymer field effect transistors (PFET) are emerging as a powerful technology option for embedding electronic functionality onto flexible plastic substrates. Applications such as flexible RFID require enhanced switching speeds from these transistors. A general guideline for improving switching characteristics of PFETs is based on the traditional MOSFET principle[1,2] where the switching-time scales as L^2/μ, (L is the channel length).[3] Major efforts have been devoted to the design and synthesis of ordered systems and in this endeavor mobility >1 $cm^2\ V^{-1}\ s^{-1}$ has been achieved for both n- and p-type transport.[4,5] In parallel, sustained efforts have been made to decrease the channel length by different lithographic[6,7] and printing techniques to obtain significantly high switching response (t_{switch}).[8] Apart from these factors, t_{switch} in PFETs is also affected by relaxation processes in the polymer dielectric layer ($t_{dielectric}$) and disorder at the semiconductor-dielectric interface ($t_{interface}$). Understanding different sources of contribution to the switching process in PFETs should enable design of high gain-bandwidth organic-circuits. In this regard, we present a comprehensive set of studies using a variety of dielectric and semiconducting layers, to arrive at a working model for the FET-dynamics. We address the limiting factors for switching and implement a strategy which enables in realizing three orders of magnitude enhancement in the response-time of these polymer devices. The highlight of this approach is that it is particularly suited for channel length regimes which come under the realm of low-cost printing methods and can be universally extended for different classes of disordered FE.

The electrical transport in PFETs is controlled by energetic- disorder and dielectric fluctuations which generally result in broadening of density of states (E_{broad}). It was recently observed that some of these issues can be mitigated with the use of polar FE dielectric.[9,10] FE dielectrics are known to form structural and energetically ordered interface with activation energy (E_A) ≈ 14 meV.[9] Additionally, FE layer in PFETs enable large transverse fields at low gate voltage (V_g) in order to observe the pinch-off (at lower V_{ds}).[3,11,12] This aspect is significant in the case of PFETs where lowering channel-length to short-channel regime introduces large deviation from ideal long-channel saturation behavior. It is generally accepted that channel length needs to be about four times the dielectric thickness to observe saturation behavior.[8] Microscopically ordered interface and high transverse field using a FE dielectric assists in improving the static and dynamic performance of PFETs. The large polarization in FE is also associated with slow response to an external time varying electric field.[13,14] This slow component of the bulk FE relaxation limits the switching response ($t_{switch} \approx t_{dielectric}$) of FE-FET, hence the fastest response obtained till-date is 0.3 ms.[15] In order to overcome this limitation, we demonstrate that poling (electric-field induced orientation) the transport interface near ferroelectric transition temperature (T_c ≈ 390 K) overcomes the slow relaxation, thereby enhancing the frequency response (ca. three orders of magnitude). Poling of FE layer is known to modify the relaxation process and the relaxation time decreases with higher magnitude of applied field.[16] This large enhancement is attributed to the fast domain nucleation process in

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DOI: 10.1002/adfm.201303374

disordered-FE and fast switching of dipoles.[16] This process is different from the switching dynamics obtained near the coercive field for ultra-thin dielectric films.[17] In case of 2-D ultra thin films the switching time increases near the coercive field. Additionally, we probe the role of microscopic dipolar heterogeneity on the dynamic response of PFETs with block co-polymer dielectrics.

We study the effect of dielectric layer polarization, interface disorder and interfacial packing of the molecular-semiconductor on the transient behavior of PFETs. Measurements were performed to emphasize the extent of contribution from all these factors. PVDF based dielectrics were used which cover a wide class from low-*k* to high-*k* paraelectrics (PE) and ferroelectrics. The transient behavior of PFETs is studied with two classes of active semiconducting materials: hole conducting rr-P3HT (*p*-FET) and high electron transporting napthalene diimide core N2200 (*n*-FET). These semiconducting polymers differ in their stacking and crystallinity at the interface.[18–20] The conjugated core of P3HT stacks close to the dielectric interface whereas in N2200 the long branched 2-octyldecyl separates the conjugated core from the dielectric interface by a distance >1 nm, thus modifying the static influence of the dielectric on the semiconductor.

Our results from a range of dielectrics and semiconductors provide a rationale and guideline for material choice and design of device structure to obtain high frequency (≈MHz) organic circuits. We present a tunable material parameter which can be used to modify the limiting processes in the switching response. Finally, with optimum material choice, improved device-dipole engineering and easy fabrication ($L \approx 20$ μm), an all-polymer-complementary inverter- circuit is demonstrated with voltage gain ~36 and switching response of 4 MHz (*β*-PVDF/N2200).

2. Results and Discussion

Bottom gate (G) top contact (S-D) FETs were fabricated on a range of dielectric and semiconducting materials. The dielectric materials were processed under conditions as described elsewhere[9] to obtain the required phase. The devices were further optimized by patterning the gate electrode and aligning it between the S-D electrodes by lithography and physical masking methods (details in the Experimental Section). The channel width (W) was 1 mm for the PFETs and L was varied over 5 μm to 250 μm range. All the PFETs were characterized by $I_{ds}(V_{ds}, V_g)$ (**Figure 1**a,b) measurement prior to studying the dynamic characteristics. Devices demonstrated distinct saturation regime which is a pre-requisite for good switching circuits. Drain current (I_{ds}) scales linearly with L, indicating negligible contact resistance (≈0.5–5% of channel resistance) in all the tested devices. More than 500 devices were tested for these studies. The results correspond to the representative mean value from the tested devices and the error bar is the mean deviation (3–5 devices) in the data set. In general, the PFETs demonstrated reliable leakage free transport with maximum hole mobility: $\mu_{FET}{}^{h} \approx 0.08$ cm^2 V^{-1} s^{-1} in case of P3HT as the active layer and maximum electron mobility of $\mu_{FET}{}^{e} \approx 0.7$ cm^2 V^{-1} s^{-1} for N2200 as the active layer. The ON-OFF ratios exhibited by the PFETs were typically in the range of 10^4–10^6.

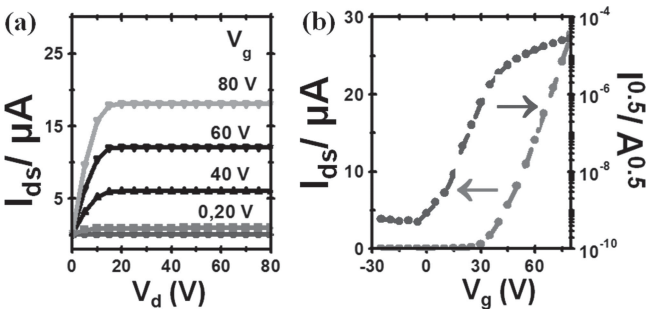

Figure 1. Typical a) I_d–V_d and b) transconductance curve obtained from n-type N2000-PFET (L = 40 μm and W = 1 mm) with *β*-PVDF dielectric layer (200 nm thickness). Detailed hysteresis and FE-FET based transconductance behavior are available in Figure S1c (Supporting Information).

These estimates of device performance are comparable to the best values reported for these polymers.[18,21]

2.1. Switching Response with Gate Pulse

Typical switching response $I_{ds}(\Delta V_g)$ obtained in response to an input square gate-pulse (ΔV_g= |40| V) for a FE-FET fabricated with N2200 semiconductor is shown in **Figure 2**. The PFET responds in sub-μs timescale. In order to extract the t_{switch} following procedure was followed: $I_{ds}(\Delta V_g)$ is monitored in the OFF state and saturation regime, corresponding to V_d = 0 V and |80| V respectively (Figure 2b). The OFF state transient originates from the parasitic capacitance of the semiconductor and dielectric due to electrode overlap and the ON state has the additional contribution of channel current. Transient profile is then depicted in terms of an effective current by taking the difference between the two recorded profiles. t_{switch} is evaluated as the time taken to completely switch on the PFET with ON/OFF ratio ≈10^5 (Figure 2c). It was ensured that the *RC* time-constant for external circuitry is 100 times lower than the response time of the PFETs (see details in the Experimental Section). The entire duration to reach the ON state (100% ≈$I_{ds,sat}$) is a preferred definition for t_{switch} rather than the standard 90% and 70% fraction, so as to include factors originating from the dielectric fluctuation processes.[22] It is known that, dielectric fluctuation processes in PFETs contributes to a slow component in the $I_{ds}(t)$ profile. The observed t_{switch} magnitudes were typically in the range of 400 ns to 100 μs and the time scales of dielectric fluctuation was significantly lower than t_{switch} (Figure 2c). Contact resistance at the metal-semiconductor interface does not affect the t_{switch} significantly. This is evident from the linear variation of I_{ds} with L and the relatively long-channel lengths (5–250) μm of the devices.

The time required for switching the transistor completely, that is, t_{switch} is determined by the carrier transit time ($t_{transit}$) between the electrodes unaffected by the interface disorder, dipole-orientation period of the dielectric layer ($t_{dielectric}$), interface energetic of the traps ($t_{interface}$) and the charging duration of the parasitic capacitors at the S-D-G overlap.[3] The time constant of the RC circuit constituted by the resistor in series with the parasitic capacitor (S-D-G overlap) for PFETs in the present study (<0.5 pF) is relatively small and its influence can

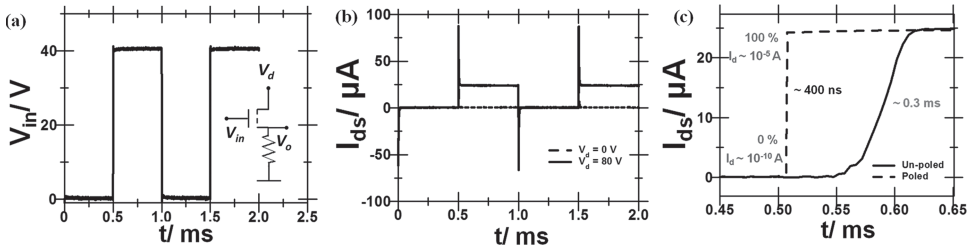

Figure 2. Switching behavior of a n-type N2200 based FE-FET (L = 20 μm and W = 1 mm) with β-PVDF (200 nm) dielectric layer in response to a square V_g pulse; a) applied input gate voltage; (inset a) circuit schematic; b) measured I_{ds} through the resistor ($R \approx$ 1–10 KΩ) at V_{ds} = 80 V and V_{ds} = 0 V; c) zoomed switching profile of I_{ds} indicating the manner in which "rise time: t_{switch}" was estimated and demonstration of the enhancement in t_{switch} after poling the interface for n-type N2200 based FE-FETs (L = 20 μm, W = 1 mm) with β-PVDF dielectric layer (200 nm).

be neglected in these measurements. We can assume a simple approximation where $t_{switch} = at_{transit} + bt_{dielectric} + ct_{interface}$, and a, b, c are weighted factors signifying the extent of contributions from each of the processes. t_{switch} variation with L for various dielectric and semiconductor combinations was obtained to understand the different processes. Typical $t_{switch}(L)$ response for different classes of semiconductors and dielectrics is shown in **Figure 3**. Expectedly, t_{switch} decreases with decrease in channel length of the PFETs, with a typical L^2 behavior. However, the L^2 behavior of t_{switch} is modified in the present case of FE-FETs, where it scales as L^{φ} with $\varphi \approx$ 1.2–1.6. This is similar to the trends observed in electrolyte and ionic liquid gated FETs.[3,23,24] Highlights of the switching response observed from different dielectrics and semiconducting polymers are as follows: i) decrease in the t_{switch} from 300 μs to 400 ns in FE-FETs upon introducing the procedure of interface poling; ii) for FE-FETs, $t_{switch}(L)$ varies as L^{φ} with $1.2 < \varphi < 1.6$ at large L and becomes independent of channel dimensions upon downscaling; iii) in case of PE-FETs, φ increases and approaches 2 with decrease in k (from α-PVDF: $k \approx$ 14 to BCB: $k \approx$ 2.6); iv) in FETs with random co-polymer (*r*-PE) like PVDF-HFP dielectrics, φ significantly varies from 1.5 in the case of *p*-FETs to 1.8–2.0 when used with *n*-FETs.

Upon introduction of poling on metal-semiconductor-FE-metal (M-S-F-M) device at $T \approx$ 370 K with a field of ± 200 MV m^{-1} (at which polarization saturation (P_s) is observed) dynamic response improves (Schematic Figure S1a, Supporting Information, details in Experimental Section). Enhancement in switching response from 300 μs to 400 ns for FE-FETs (β-PVDF/N2200, L = 20 μm) is evident upon comparing pre-poled and un-poled interfaces as shown in Figure 2c. We analyze this poling induced enhancement in switching response in terms of the intrinsic domain dynamics of FE-dielectric. In a polymer-FE dielectric the total time for polarization switching is governed by nucleation limited switching (NLS) which involves $t_{nucleation}$ the time taken for domain nucleation, $t_{relaxation}$ the response of the domains (dipoles thereof) to the field, that is, $t_{dielectric,FE} = t_{nucleation} + t_{relaxation}$. Typically it is seen that the domain nucleation is the slowest step.[25] Once the nucleation of domains occurs, further alignment and orientation is relatively fast due to the co-operative dipole motion in FE-dielectrics. The initial bias applied to the M-S-F-M overcomes the slow domain nucleation step and $t_{dielectric,FE} \approx t_{relaxation}$. Hence, faster switching speeds are obtained for FE-FETs with pre-poled interfaces. This enhanced switching behavior due to the poling process is sustained till ≈10^4 min when the device is continuously operated at 300 K under ΔV_g = 80 V or 40 V and V_{ds} = 80 V D.C. It is also observed that poling for shorter duration does not complete the nucleation process and is reflected by a slow component in the switching profile as shown in Figure S1b, Supporting Information. Thus, the switching profiles of FE-FETs can be tuned by parameters such as bias-magnitude, poling-duration and temperature. It should be mentioned that FE-FETs (N2200 active layer, β-PVDF dielectric layer, L = 20 μm and W = 1 mm) fabricated using un-poled dielectrics typically exhibited slower response (≈0.3 ms) similar to the earlier reported results.[15] This method of enhancing the polarization time by pre-poling can be applied for other classes of disordered FE films like lead zirconate titanate (PZT) which also follows the NLS mechanism.[26,27]

Impedance spectroscopy was performed on M-I-M capacitors (200 nm thick dielectric layer) with different dielectrics to

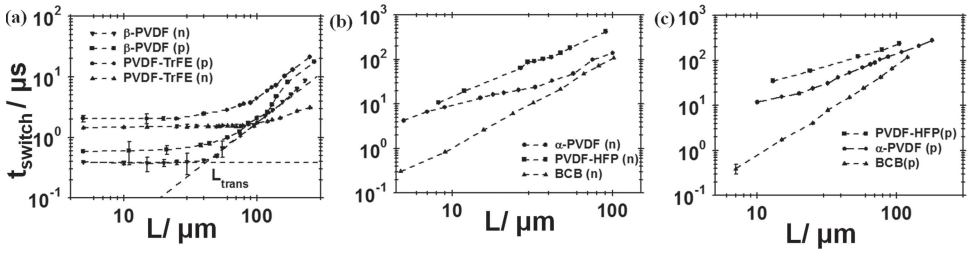

Figure 3. $t_{switch}(L)$ in log–log scale for n-FETs (n) and p- FETs (p) with a) FE dielectric and b,c) PE dielectric layers. Error bars indicate the mean deviation obtained from (3–5) devices at each channel length. For the sake of appropriate comparison across different class of materials, the thickness of dielectric and semiconducting layers were in the narrow range (200 ± 10) nm and (50 ± 5) nm respectively and W is 1 mm for all devices. In all the devices, parasitic capacitance from the electrode overlap was maintained at 0.5 pF.

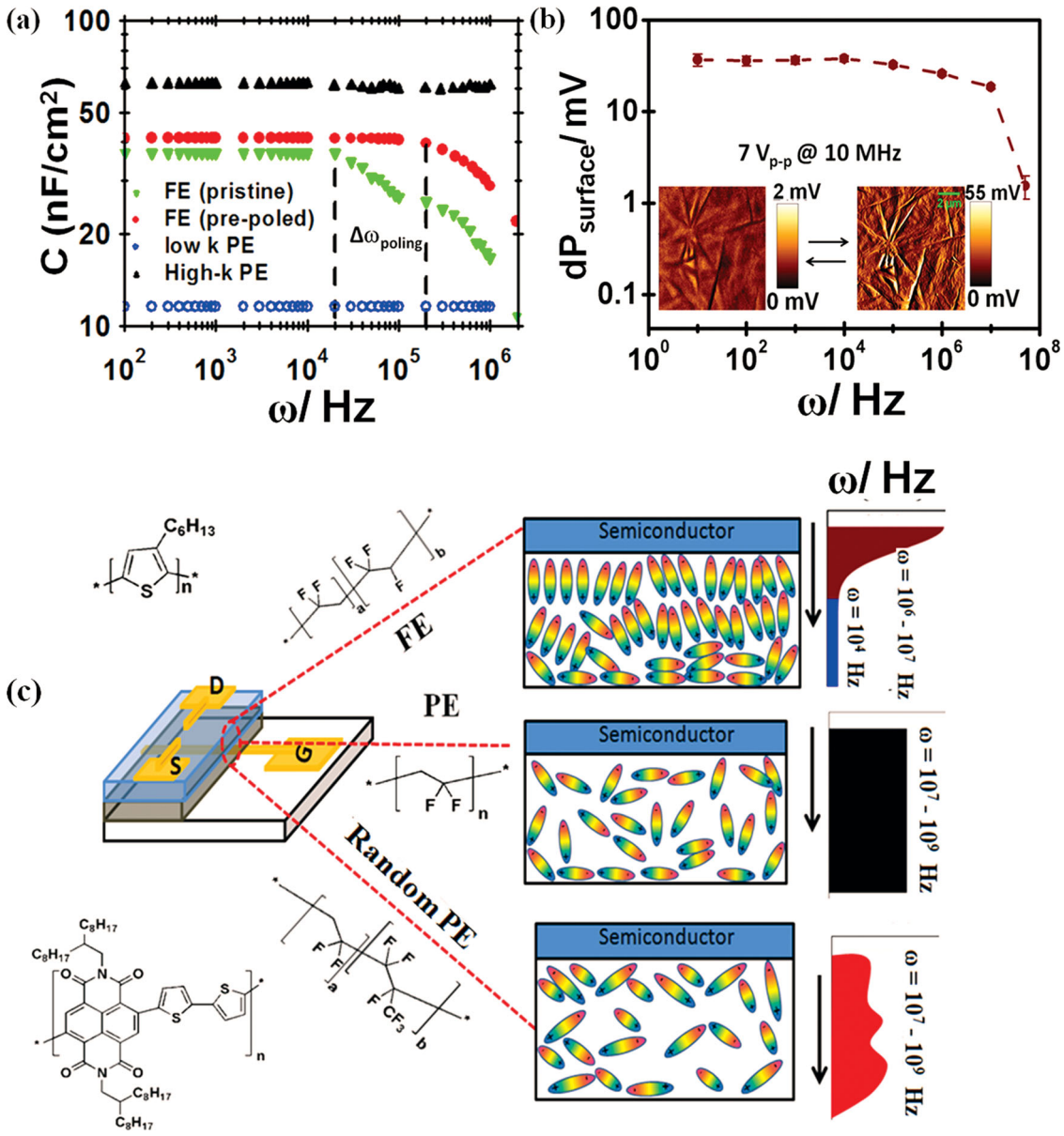

Figure 4. Impedance spectroscopy of dielectrics and the effect of poling on the frequency response. a) Bulk capacitance response from M-I-M devices for different dielectric layers (200 nm), $\Delta\omega_{poling}$ represents the change in frequency response of FE layer upon poling; b) measurement of polarization contrast with frequency from SCM spectroscopy. Finite value of the polarization contrast indicates the surface dipoles can respond to that frequency. Inset (b) is the representative polarization contrast (at 10 MHz) obtained from SCM measurements for PVDF-TrFE layer (200 nm) coated on ITO (details in Experimental Section and Supporting Information,S2b). c) $k(\omega)$ behavior along the thickness for different dielectrics and the structure of the dielectric and polymers used.

probe the bulk dipole dynamics. In the case of high-k PE and low-k dielectrics, bulk capacitance (C) is largely independent of ω in the 100 Hz–1MHz range (**Figure 4**a). However, in the case of FE capacitors (PVDF-TrFE), C is ω dependent and perceptibly decreases beyond 10^4 Hz. Upon applying the poling procedure, the ω-range extends beyond 10^5 Hz (Figure 4a). The extent over which the magnitude of $C(\omega)$ is effective, determines the limit of the switching response for pre-poled FE-FETs. Additionally, in the case of FE dielectrics the surface dipoles contribute a significant fraction to the net polarization (Figure S2a, Supporting Information). The surface dynamics of the pre-poled FE layer is relatively fast and can be quantified by scanning capacitance microscopy (SCM) measurements (Figure 4b, see details in Experimental Section and Supporting Information S2). SCM measurements show that the surface impedance response of these poled FE films extends upto ≈10 MHz (Figure 4b). Hence, a distribution in the frequency response from 10^5 in the bulk to 10^7 in surface exists along the cross-section of the pre-poled FE layers (Figure 4c). The polarization response of a FE-FET originates from the linear combination of $C(\omega)$ behavior from different layers.

In addition, we observe a transition in switching response of FE-FETs (with L) from power-law behavior to L independent

behavior. t_{switch} being independent of L essentially implies that the switching response in this regime is controlled by the dielectric relaxation (i.e., $t_{switch} \approx t_{dielectric}$) and not by the transit of charge carriers. We define this transition channel length (L_{trans}) as the length where the transport time of charge carriers in the channel equals the dielectric relaxation. L_{trans} was obtained to be 25 μm in the case of PVDF-TrFE and 20 μm for β-PVDF based *n*-FETs (Figure 3a). Above L_{trans}, $t_{switch}(L)$ takes on a power law behavior and at sufficiently large L, t_{switch} can be expressed as an approximate sum of separate processes; $t_{switch} = at_{transit} + bt_{dielectric} + ct_{interface}$ ($t_{interface} << t_{transit}$ or $t_{dielectric}$). If the criterion of switching is specified to the 90% and 70% magnitude, then L_{trans} assumes a low value of < 5 μm. Similar transition was also observed in the frequency domain analysis for FE-FETs which is obtained from a direct measurement of current gain of the PFETs (details in Supporting Information S3).

It was observed that the exponent φ, obtained from $t_{switch} \sim L^{\varphi}$ can be tuned by modifying the crystallinity of the FE layer (PVDF-TrFE). The crystallinity is estimated from the relative peak intensity of β-phase from FTIR and XRD. FE-FETs fabricated with varied crystallinity (95% at annealing condition of 140 °C to 50% when annealed at 90 °C) of the FE-layer also followed similar trend in $t_{switch}(L)$ as seen in Figure 3a. However, a higher value of L_{trans} and slower response is obtained from these devices. It is known that switching of FE without domains is generally a slower process due to the absence of co-operative motion.[25,28] Hence, the slow response for FE layers with low crystallinity originates from: i) combination of relaxation dynamics of differently aligned domains and grain boundaries; and ii) slower dipole relaxation processes in the sizable amorphous regions. In addition as the crystallinity of PVDF-TrFE layer in FE-FET decreases, the exponent φ in the $t_{switch}(L)$ dependence reduces from 1.6 to 1.4 (Figure S4, Supporting Information). The physical interpretation of φ as a measure of dielectric order and not from parameters like contact resistance can then be justified based on this trend.

It is also observed that, in the regime where t_{switch} is controlled by $t_{dielectric}$ the dynamic behavior can be modified by the top molecular semiconductor layer. FE-FETs fabricated from β-PVDF dielectric layer with $L \approx 5$ μm ($<L_{trans}$), showed an increase in t_{switch} from 400 ns to 600 ns when the polymer layer is changed from N2200 to P3HT. This trend can be attributed to the characteristic molecular packing of the semiconductor on the dielectric surface. It is known that the introduction of semiconducting layer on a FE induces depolarization[9,29] which disrupts the ordered and co-operative dipoles of the FE (Supporting Information S5). Isolation of the polymer conjugated core from the dielectric interface minimizes the depolarization and co-operative response of FE is retained to obtain better t_{switch}. In general, our results point to the fact that molecules with isolated core and face-on arrangement should be preferred for fast switching.

For PE dielectrics (α- PVDF), t_{switch} could be fitted with exponent $\varphi \approx 2$ in the complete range of L for both n-FETs and p-FETs as shown in Figure 3b,c. Devices fabricated from these dielectrics have characteristic time scales as: $t_{dielectric}$ (10^9 Hz) << $t_{transit}$ and $t_{switch} \approx t_{transit} + t_{interface}$ (for $L \geq 5$ μm). In general, t_{switch} for high-k PE based PFETs is higher than pre-poled FE-FETs. This behavior can be directly correlated to the ordered interface obtained with FE dielectrics compared to high-k PE-FETs. Additionally, even though the magnitude of k does not vary significantly between PVDF-HFP ($k \approx 13.5$) and α-PVDF ($k \approx 14$), the switching response for PVDF-HFP ($t_{switch} \approx 250$ μs) based *p*-FETs is observed to be slower than α-PVDF ($t_{switch} \approx 120$ μs). This behavior can also be attributed to the heterogeneous molecular dipoles in *r*-PE with different response time. These random dipoles can substantially contribute to the interface disorder affecting the charge transport and the associated dynamics (detailed analysis of interface contribution to the dynamic response is in **section 2.3** of main text). Additional clue for the dominance of interface dynamics in the switching response of PFETs fabricated with *r*-PE dielectric layer comes from different values of exponent φ for different semiconductors. φ attains a value of 1.8–2 for N2200 whereas it is takes a value of 1.5 for P3HT based PFETs. This is because in N2200 the conjugated core is decoupled from the dielectric. Hence switching in *n*-FETs is weakly affected by the interface disorder from the dielectric layer compared to *p*-FETs. These analyses highlight the inherent differences in the transient response for various classes of dielectrics and semiconductors.

2.2. Temperature Dependent Gate Pulsed Switching

$t_{switch}(T)$ provides considerable insights into the switching mechanism (**Figure 5**). These measurements were performed for FE-FETs (Figure 5a,b) with channel lengths of $L > L_{trans}$ and $L < L_{trans}$ as well as for PE-FETs (Figure 5c). In the case of PE-FETs where the dielectric layer plays a minimal role, $t_{switch}(T)$ exhibits an activated behavior and is identical to $\mu_{FET}(T)$.[9] This indicates that the switching in these PFETs is transport limited (i.e., $t_{switch} \approx t_{transit}$). The magnitude of E_A estimated from

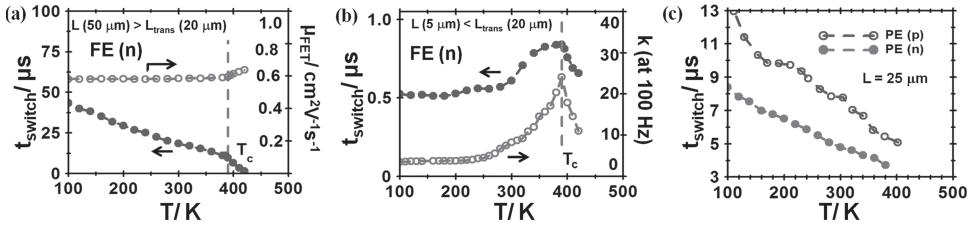

Figure 5. Static and dynamic characteristic variation with T for FE-FETs and PE-FETs revealing the crossover behavior in switching mechanism. a) $t_{switch}(T)$ and $\mu_{FET}(T)$ for n-type N2200 based FE-FETs with PVDF-TrFE dielectric (200 nm). b) Small channel ($L \approx 5$ μm), $t_{switch}(T)$ response for FE-FETs from N2200 semiconducting layer (50 nm); also shown is the $k(T)$ behavior for PVDF-TrFE in M-I-M structure. c) $t_{switch}(T)$ for n-type (N2200) and p-type (P3HT) active layer with α-PVDF (200 nm) dielectric. T_c (390 K) indicates the FE-PE phase transition in PVDF-TrFE.

$t_{switch}(T)$ for N2200 devices is in the range of 47–62 meV and is marginally lower than that of P3HT based devices (81–120 meV) (Figure 5c). In case of FETs fabricated with *r*-PE dielectric layer, the observed lower t_{switch} originates from low mobility which translates to a higher magnitude of $E_A \approx 150$ meV (PVDF-HFP/P3HT based PFETs)

Interestingly, the device response of FE-FETs varies significantly with channel length for both *n*-FETs and *p*-FETs. For devices with $L > L_{trans}$, $t_{switch}(T)$ follows an activated behavior similar to that of $\mu_{FET}(T)$ with low magnitude of $E_A \approx 14$ meV (Figure 5a).[30] However, in the devices with $L < L_{trans}$, $t_{switch}(T)$ follows a quadratic trend similar to $k(T)$ behavior (Figure 5b, Supporting Information S6). This proves that for FE-FETs with small L ($<L_{trans}$), the switching dynamics is primarily controlled by slow dielectric relaxation. It is also observed that beyond the phase transition of PVDF-TrFE from FE to PE phase at $T > T_c$, $t_{switch}(T)$ becomes activated for all L values with $E_A \approx 0.4$ eV. These T dependent measurements gives clear evidence of change in switching mechanism for FE-FETs from dielectric limited processes to semiconductor transport limited process.

2.3. Transient Response from Drain Pulse

Drain pulse voltage in the presence of finite V_g introduces a transient drain current with characteristic profiles which depend on the transport mechanisms. The presence of V_g ensures that the dielectric factors minimally contribute to the transient response. Typical drain-transient profile in response to a square-drain-pulse is shown in **Figure 6**a (β-PVDF/N2200 based PFET). The transient switching time (t_{ds}) is obtained from the effective drain current by taking the difference between the two recorded profiles obtained in the ON ($V_g = 80$ V) and OFF state ($V_g = 0$ V) of the PFET in the presence of a pulsed $\Delta V_{ds} = |80|$ V or $|40|$ V.

The time required for switching-on the drain current at a constant V_g is determined by the transit delay time of charge carriers ($t_{transit}$) and the charging duration of the semiconductor sheet capacitor governed by the interface conductivity.[31,32] Simulation of the dynamic electric field distribution in the device during the transient measurement is shown in Figure S7. This dynamic response is arrived at by solving the Poisson's equation and drift-diffusion under appropriate boundary conditions of an operating FET (Supporting Information S7). Complete analysis of the dynamic response obtained from varied V_{ds} and V_g brings out the factors contributing to t_{ds}. In a simplistic approach, $t_{ds} \approx t_{transit} + t_{interface}$ with appropriate weighted factor for each process (details in Supporting Information S8).

To distinguish the interface dynamics of different dielectrics and semiconductors, t_{ds} was measured with varying channel lengths (Figure 6b) and fitted as a power law ($L\delta$). It is expected that $t_{ds} \sim L^2$ for devices involving lateral transit of charge carriers.[33] If the introduction of dielectric layer (of PFET) does not significantly affect the lateral transport in the semiconductor then the square law behavior is retained. So, PFETs fabricated from low k dielectrics with an ordered interface follow L^2 dependence. Similarly, in the case of FE-FETs with ordered transport interface ($E_A = 14$ meV for PVDF-TrFE/P3HT transistor) typical L^2 response is obtained. However, if the dielectric layer introduces disorder in the semiconductor, deviation from L^2 behavior is obtained. $t_{ds}(L)$ indicated a trend of lower δ value with increase in k of the dielectric layer and lowest value of δ (≈1.6) was obtained for PFETs using *r*-PE as dielectric layer. Additionally, it was also seen that treatment of SAM layer like HMDS on the dielectric surface modifies the interface and δ increases (from 1.5 to 1.7 for *r*-PE/P3HT devices). These measurements indicate that the value of δ is a measure of disorder at the interface with lower value implying higher degree of interface disorder. This can be attributed to the fact that as L increases the spatial access to disordered sites in the semiconductor increases. Hence, more traps needs to be filled up to attain channel conduction. So for a disordered interface weaker dependence of L is obtained. Activation energy ($E_{A,DC}$) estimation independently done from the T dependent DC transconductance measurement follows the trend similar to the variation of the parameter δ (Figure S9a,b, Supporting Information). Low δ value for *r*-PE based PFETs indicates the effect of heterogeneous polar environment at the transport interface. All the above observations corroborates that the variation of δ has no contribution from geometric parameters due to electrode overlap or contact resistance rather correlates directly to the interface energetics.

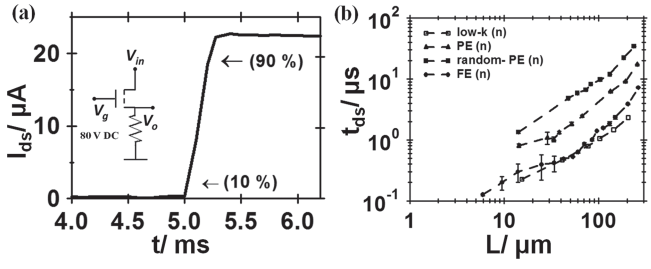

Figure 6. Drain transient response (t_{ds}) for different dielectrics in n-FETs. a) Typical response for N2200 based FE-FET ($L = 60$ μm and $W = 1$ mm) with β-PVDF dielectric layer (200 nm). Inset shows the circuit diagram. b) $t_{ds}(L)$ for n-FETs fabricated from different dielectric layers. Parasitic capacitance from the electrode overlap was maintained at ≈ (0.5 ± 0.1) pF for all L values and $W = 1$ mm for all devices. Error bars indicate the mean deviation obtained from (3–5) devices at each channel length. Similar analysis was performed for p-FETs with P3HT as active layer.

2.4. Analysis of Interface Parameters

Further insight into the wide range of results can be adjudged by the exponent-parameter φ (obtained in Section 2.1: $t_{switch} \sim L^{\varphi}$) whose magnitude is indicative of the limiting processes. Our analysis shows that φ is dependent on μ_{FET}, $E_A(\delta)$, and $\omega_{dielectric}$, ($=1/t_{dielectric}$) as shown in **Figure 7**. The trends in φ over a range of materials can map the dynamic response of PFETs. The comparison of parameters obtained from dynamic measurements with parameters like E_A and μ_{FET} obtained from standard transconductance measurements is instructive. Empirically, $t_{transit}$ and $t_{interface}$ can be expressed as, $t_{transit} \approx \frac{2\pi L^2}{\mu FET Vd}$ and $t_{interface} \approx \frac{2\pi L^{\delta}}{k'(\chi+1)(V_g - V_t)^{2\chi} V_d}$, where k' is related to the ease of hopping, ξ is related to the characteristic temperature T_0 which gives the broadening of density of states (see details in Supporting Information S10).

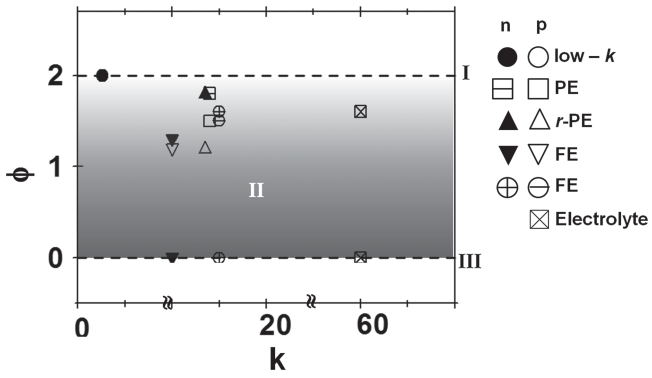

Figure 7. Universal map of dynamic response from the plot of parameter φ (extracted from $t_{switch} \sim L^{\varphi}$) for different materials. Regime I ($\varphi = 2$) corresponds to semiconductor transport limited dynamics ($t_{switch} \approx t_{transit}$), regime III ($\varphi = 0$) corresponds to dielectric relaxation limited switching mechanism ($t_{switch} \approx t_{dielectric}$), region II ($1 < \varphi < 2$) corresponds to the contribution from all the factors ($t_{switch} = at_{transit} + bt_{dielectric} + ct_{interface}$). Error bars indicate mean deviation from 3 sets of measurements. n and p represent data points for n-FET and p-FET respectively. Electrolyte response is obtained from the literature.[3]

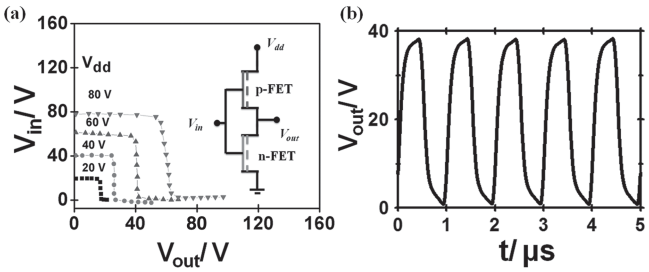

Figure 8. Static and dynamic characterization of polymer inverters (L = 5 µm and W = 1 mm) with N2200 (50 nm) based n-FETs as load and P3HT (50 nm) based p-FETs as driver. a) Typical transfer voltage curve with β-PVDF (200 nm) as the dielectric layer. Inset shows the schematic electrical connections. b) Switching response of the same inverter at input frequency (ω_{in}) of 1 MHz and V_{dd} = 40 V. These curves represent that the devices can be operated at even higher frequency. Similar curves were also obtained from different dielectrics and also with p-FETs as load (Supporting Information S11).

$t_{switch}(L)$ for PE-FETs was fitted using k' and χ as free parameters (**Table 1**). These parameters yield an effective wave-function overlap of 0.1–0.4 nm and T_0 value (proportional to the broadening of DOS) in the range of 360–525 K. E_A and μ_{FET} values obtained from standard transconductance measurements follow the trends of the parameters obtained from the dynamic measurements and is consistent with the interpretation of the time domain studies [34,35] (Table 1 and Supporting Information S10).

Optimized device geometry and interface parameters were utilized to obtain all-polymer complementary circuits (details in Supporting Information S11) operating at 4 MHz frequency (**Figure 8**). Frequency response of inverters was determined by applying input pulses of different frequencies. Maximum operating frequency is determined as the frequency till which output follows the input. Such high frequency response (≈4 MHz) for all-polymer logic circuits is the best response obtained till date and opens up opportunities for more complex electronic archeitectures with polymers.

Table 1. Parameters extracted from fitting of t_{switch} (L) and transconductance measurements of PFETs with different dielectrics and semiconductors. k' and χ which are related to interfacial properties are extracted from dynamic measurements which match E_A and μ_{FET} obtained from DC transconductance measurements.

Polymer	Dielectric	$k' \times 10^{-9}$ [cm^2 s^{-1}]	χ	E_A [me V]	μ_{FET} (at 300 K) [cm^2 V^{-1} s^{-1}]
P3HT	BCB	4.48	1.25	56	0.08
	α-PVDF	1.16	1.66	86	0.014
	PVDF-HFP	0.632	1.75	116	0.04
N2200	BCB	6.57	1.2	45	0.5
	α-PVDF	2.07	1.46	60	0.12
	PVDF-HFP	1.84	1.5	63	0.15

3. Conclusion

In conclusion, systematic control and enhancement in the switching response in PFETs is demonstrated by dipole and device engineering. PFETs capable of operating at 400 ns switching-speed are obtained at printable long channel lengths using FE dielectric. This was possible due to a combination of factors including high transverse field, ordered interface and co-operative dipole switching in FE-dielectrics. Drain transient measurements, AC analysis and T dependent behavior was used to understand the limiting processes and distinguish different switching mechanisms. Significant correlation is found between the switching characteristics of PFETs and various microscopic relaxation and transport processes. Polymers with higher conductivity and isolated conjugated core as well as dielectrics with ordered dipoles and disorder free interface satisfy the pre-requisites for fast switching circuits. Upon implementing these specific strategies, we demonstrate low-voltage all polymer complementary logic circuits with switching frequency >1 MHz. Our studies broaden the utility of disordered FE dielectrics to obtain faster circuits and opens up opportunities to realize the full potential of flexible and printable electronics.

4. Experimental Section

Materials: Conjugated polymers rr-P3HT (weight average molecular weight, $M_w \approx 87\,000$) was procured from American Dye Source Inc. and P(NDI2OD-T2) from Polyera Corporation USA. Dielectric materials PVDF ($M_w \approx 180\,000$); PVDF-HFP copolymer ($M_w \approx 455\,000$), PVDF-TrFE (75/25) and (BCB) were obtained from Sigma Aldrich Inc., Measurement Specialties Inc., USA and Dow Chemicals respectively.

FET: Bottom gated top contact FETs were fabricated by coating patterned electrode-Al or Cr/Au (10^{-6} mbar, 1 Å s^{-1} , 30 nm thick) with shadow mask on glass substrates. Dielectric materials of thickness ≈200 nm were coated by procedure described elsewhere to result in desired phases.[9] Polymer active layers rr-P3HT and N2200 (50 nm thick) were coated from a solution of 10 mg mL^{-1} in chlorobenzene at 1000 rpm. P3HT films were annealed at 110 °C for 30 min and N2200 films at 110 °C for 2 h. This was followed by the deposition of S-D patterned-aligned electrodes by shadow masking technique. Devices were fabricated with L varying from (5–250) µm and W = 1 mm.

DC Measurements: Current–voltage characteristics of the PFETs were measured with Keithley 4200 SCS. Capacitance measurement was performed at 100 Hz using HP4294A.

Switching Measurement: A train of square voltage pulse (±80 V or ± 40 V for n-FET and p-FET respectively) was applied at the gate with an arbitrary waveform generator (K-Pulse Card Keithley or SMU) while the drain electrode was held at a DC bias (0 or ± 80 V using Keithley 2400). The transistor switching speed was measured by monitoring the voltage drop (inset in Figure 2a) over a resistor ($R \approx$ 1–10 kΩ depending on the channel length), between the source electrode and ground, using an oscilloscope (Lecroy 6100A). The input capacitance of our set up (Lecroy 6100A with RF probes) was <5.5 pF with RC time constant ≈5 ns. To obtain the drain transient response square pulses (± 80 V or ± 40 V) were applied at the drain end and voltage at the resistor ($R \approx 0.1 - 5$ kΩ) between the source and ground was monitored (inset in Figure 6a) while keeping the bias at the gate electrode constant (0 or ± 80 V).

Interface Poling: In case of FE-FETs, the semiconductor films coated on dielectrics were biased at ± 40 V (for dielectric films of thickness 200 nm) with gold coated PDMS soft contacts for 30 minutes at T ~ 370 K in vacuum before the coating of the S-D electrode. 40 V was chosen as the bias voltage since it corresponds to the field at which P_s for FE-films of 200 nm thickness is observed. PDMS soft contacts were prepared by coating 1 μm thick gold film on (2–3) mm free standing PDMS substrate. Device with the FE and semiconducting layer was clipped with PDMS contacts completing the M-F-S-M structure (Schematic in Figure S1a, Supporting Information). It was ensured that the M-F-S-M structures were in accumulation mode with bias. The domain nucleation and growth rates were monitored and optimized by trials. Extent of domain nucleation in the FE layer could be tuned by varying the applied voltage, *T*, and duration of bias (Figure S1b, Supporting Information).

SCM: Dielectric films grown on ITO coated transparent substrates were used for SCM characterization. Surface capacitance of the sample is obtained by using a Cr/Pt coated conducting tip (Multi-75E, Resonant frequency, ω_R = 75 kHz) which senses force proportional to dC/dz. SCM retrace measures the capacitive force using lock-in amplitude at ω_R, while tip is driven at $\omega_R/2$ in hover mode (40 nm). To estimate the dipole response poling of dielectric surface was performed using an in-built sinusoidal source (7 $V_{p\text{-}p}$) in the range of 100 Hz to 50 MHz applied through the tip. The connections to the device was impedance matched till 2 GHz. SCM is then performed on the biased area to measure the difference of force or the surface capacitance with poling and obtain the average polarization contrast (dP). Frequency response of the surface dipoles is obtained as the frequency at which $\frac{dP}{d\omega}$ undergoes a slope change (Figure 4b).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

S.P.S. acknowledges CSIR, India for fellowship and K.S.N. acknowledges DAE-India for funding.

Received: September 30, 2013
Revised: December 18, 2013
Published online: February 10, 2014

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